

FIG.2

1	FADD FR0 , FR1	; FPU INSTRUCTION	1
2	ADD R0 , R1	; CPU INSTRUCTION	1
3	SUB R2 , R3	; CPU INSTRUCTION	2
4	FDIV FR2 , FR3	; FPU INSTRUCTION	2
5	SHAD R4 , R5	; CPU INSTRUCTION	3
6	OR R6 , R7	; CPU INSTRUCTION	4

FIG.3

1	FADD FR0 , FR1	; FPU INSTRUCTION	1
2	NOP	; CPU INSTRUCTION	1
3	NOP	; CPU INSTRUCTION	2
4	FDIV FR2 , FR3	; FPU INSTRUCTION	2
5	NOP	; CPU INSTRUCTION	3
6	NOP	; CPU INSTRUCTION	4

FIG.4

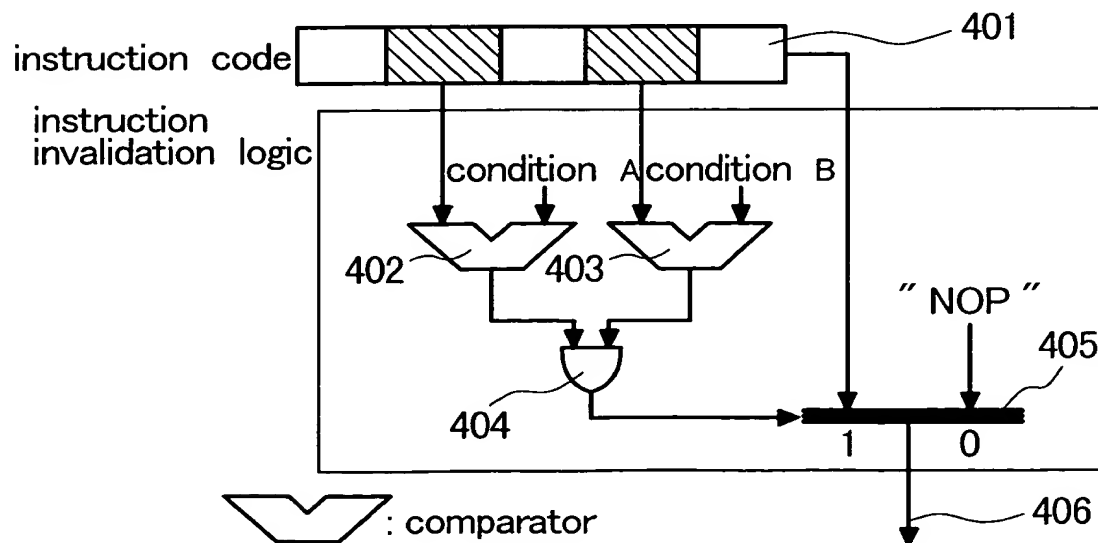


FIG.5

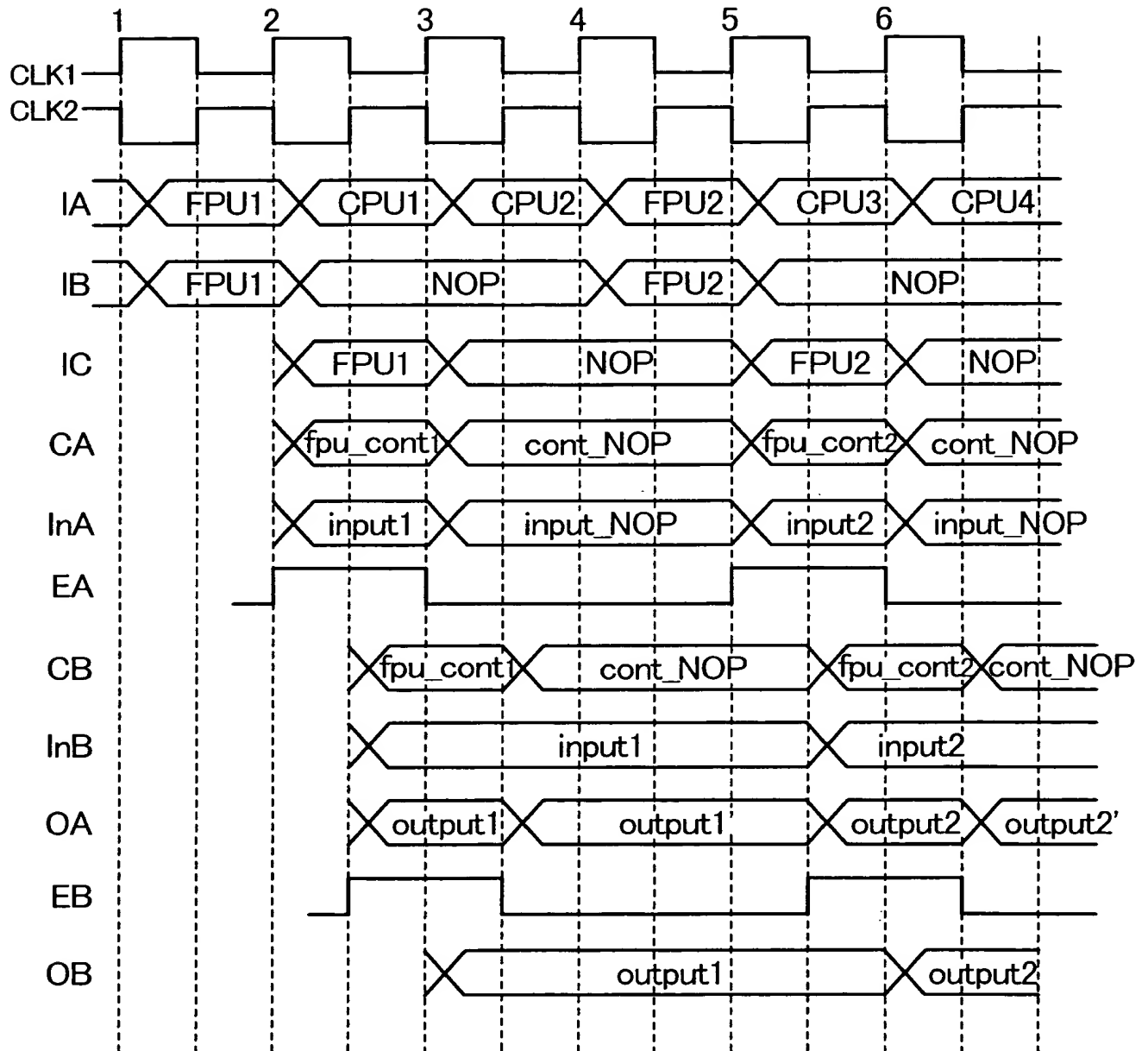


FIG.6

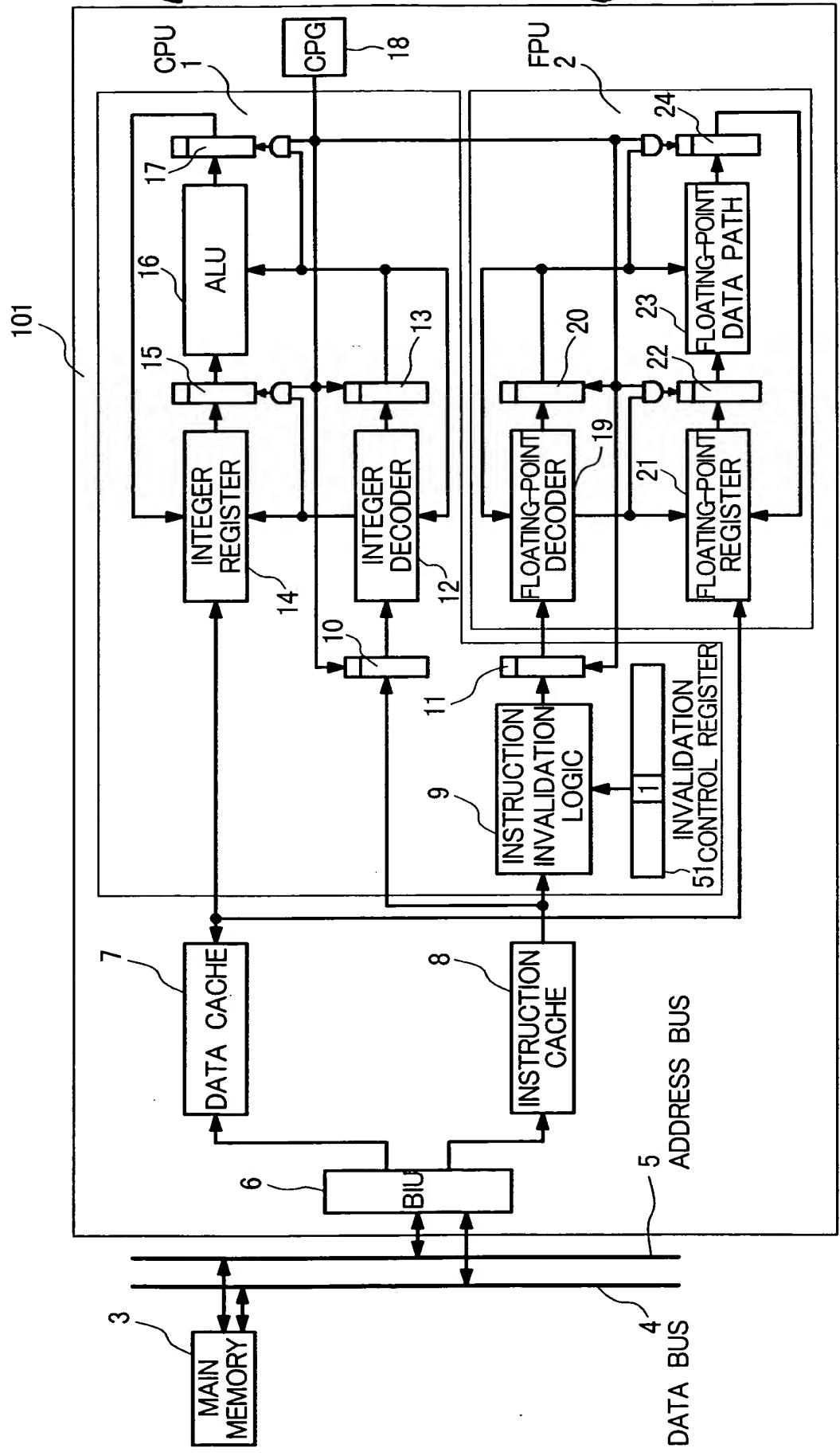
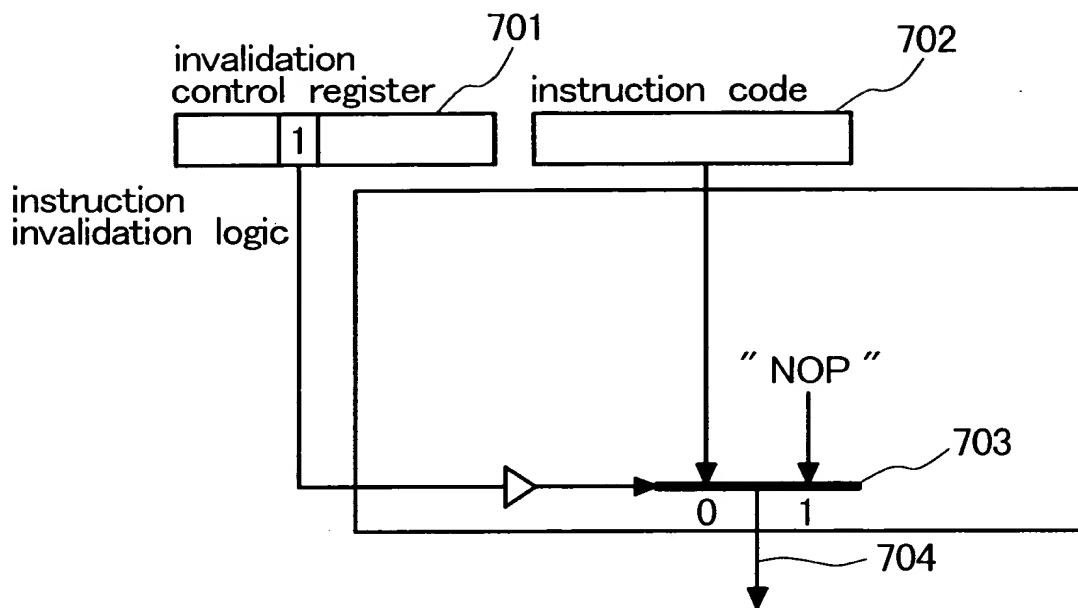


FIG.7



[illegible]